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Patents ADP number *(if you know it)*

7443872001

If the applicant is a corporate body, give the country/state of its incorporation **GB**

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Arbitration Management Method and System

5. Name of your agent *(if you have one)*

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DUPLICATE

Arbitration Management Method and System

FIELD OF INVENTION

This invention relates to an arbitration management method for use in identification systems, more particularly, but not exclusively, in RFID systems. There is provided a method of identifying a plurality of transponders each of which transmits data at intervals to a receiver. The invention also relates to an identification system comprising a plurality of transponders and a receiver, to the transponders themselves and to an integrated circuit for use in a transponder.

BACKGROUND TO THE INVENTION

Identification systems are known in which a plurality of transmitters, typically transponders (commonly called tags), are activated by a power signal (or an "interrogation signal") and then transmit signals, usually containing identification data to a receiver, which typically forms part of the interrogator. The signals may be transmitted in many ways, including electromagnetic energy, eg. radio frequency (RF), infra red (IR), coherent light and sound, eg. ultra-sound. For example the transmission may be achieved by actual emission of RF energy by the transponders, or by the modulation of the reflectivity of an antenna of the transponder, resulting in varying amounts of RF energy in the interrogation signal being reflected or back-scattered from the transponder antenna.

Radio Frequency Identification systems are used to remotely identify, take a census of, locate or otherwise interact with people, objects or groups or clusters of people or objects. The systems usually comprise interrogators also known as readers, and transponders also known as tags.

It is not usually a problem for a reader to communicate with a single tag which is presented to the reader, such as in an access control system. However in the situation where many tags may be present in a reader's field of views, such as a crowd of people, or a pallet load of goods having tags attached, the transmissions by the tags would occur together and cause collisions, rendering the transmissions unusable due to mutual interference. A number of arbitration methods have been developed to enable a reader to sort and/or isolate and transact with these large populations of tags. These methods are known variously as anti-collision schemes or collision-arbitration algorithms.

In one example described in US 5,537,105 (corresponding to EP 494114 B1) by Marsh et al, the whole contents of which are incorporated herein, the transponders on receipt of an interrogation signal repeatedly transmit a response signal containing data which identifies the transponder. The interrogator detects successful identification of any transponder and briefly modifies the interrogation signal to indicate the successful identification. Each transponder includes a logic circuit responsive to a respective modification in the interrogation signal to cease transmission of its own response signal. The response signals are transmitted at random intervals until the identity of a transponder is successfully read and acknowledged by the reader and placed into a dormant or gagged state. US5699066 (corresponding to EP0585132) and PCT application GB98/01385 (corresponding to WO/985142) also describe methods in which the response signals are transmitted at pseudo-random intervals. The whole contents of EP0585132 and WO/985142 are incorporated herein by reference.

Other examples of such methods are described in US5699096, Cole WO 01/41043 A1, and Maletsky US6104279.

Methods have been used to improve the randomness of the response intervals. In EP 467036 B1, the whole contents of which are herein incorporated, the identification system uses a pseudo-random delay between transponder data transmissions. In this example, a linear recursive sequence generator is seeded by the transponder identification address to provide the pseudo-random delay between tag data transmissions. US5550547 describes a similar system in which the tag sends out a 64 bit ID code at intervals determined by a random number generator. US6104279 describes a system in which remote units re-transmit their bit pattern at random intervals. It further mentions that there are many techniques to produce a random number; for example the identification number can provide the seed for a random number generator permitting the user to individually seed each tag with a different random number.

Another method is based on slotted polling or slotted Aloha schemes in which tags randomly select a time slot in which to transmit and then transmit when it is their turn to do so. The theory is that because slots are randomly selected, sooner or later all tags will have had the opportunity to transmit messages 'in the clear'. WO 01/41043 describes such a system in which RFID tags randomly select a slot in which to transmit. In a practical implementation the slot selection by a tag is made on a pseudo-random basis, using a seed for a random number generator, which is derived

from either part of the data held on the tag or by pre-programming a seed where the tag is manufactured. The possibility is great that many tags will have the same slot allocation choice. The fewer the number of slots to choose from, the greater will be the probability that many tags will 'randomly' select the same slot time and so will always collide and will therefore never be successfully read.

Patent Application WO9926081, the whole of which is included herein by reference, describes a method and system for improving the reading efficiency of slotted systems by optimising the maximum waiting time before a tag (transponder) transmits or adjusts the number of slots over which a tag may randomly choose to transmit its reply. If there are too many tags in the field and the congestion is heavy, the maximum waiting time may be increased or the number of slots may be increased to relieve this congestion. The converse is also true; if there are few tags in the field and there is little or no congestion, the maximum waiting time may be decreased or the number of slots may be decreased in order to improve overall throughput. A Tag (Transponder) may dynamically alter the waiting time or number of slots over which it randomly transmits in response to an instruction from the interrogator. Alternatively, the tags (transponders) may be adapted to detect either heavy or light congestion and adjust their waiting time or slot number accordingly. Tags may increment or decrement their wait time or number of slots in increments in a number of stages or alter to any length for example number of clock pulses. The alteration of the waiting period imposes no limitation on the technique which may be used to determine the waiting time or number slots. When referring to time slots, a number of time slots are arranged in groups representing the maximum waiting time. These groups are usually referred to as Rounds. The number of time intervals contained within a maximum hold-off period can therefore be referred to as the Round Size.

Prior art systems use complex methods with fairly large logic circuits to store the Round Size value and required the slot counter to be electrically "re-wired" in order to change the count value. This results in increased chip size and power consumption.

One object of the present invention is striving to provide simpler methods of adjusting the Round Size so as to decrease chip complexity, enhance simpler operation and reduce power consumption which translates into longer read ranges.

SUMMARY OF THE INVENTION

According to one aspect of the present invention there is provided a method of identifying a plurality of transponders in an interrogation process comprising transmitting an interrogation signal to the transponders and receiving a response signal from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted, characterised by creating a plurality of data line signals together defining a random number, feeding said data line signals to a counter for determining the waiting period, and providing at least one of the data lines with logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

In one embodiment the transponder uses a random or pseudo-random number generator to derive the random number, transmitting output signals from the random or pseudo-random number generator to respective inputs of the counter for determining the waiting period. Hereinafter the term "random number generator" will be used to include either a random number generator or a pseudo-random number generator.

The logic circuitry may comprise one or more logic gates, for example AND gates, the number of logic gates preferably being less than the number of data lines.

The waiting period typically consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period. There is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used. In a binary system the maximum duration of the waiting period is increased or decreased by multiples of 2 or 0.5 respectively. Therefore, the desired Round Size is selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

In one embodiment the step of clocking the random number generator and/or clocking the counter is by means of a clock oscillator of the transponder. The transponder transmits an output signal, from its transmitter when the counter has been counted to its terminal count, the output signal being

triggered by a trigger signal from the counter, the trigger signal also triggering the counter to load a fresh or new number from the random number generator for the next count.

The maximum possible waiting time or maximum possible number of slots over which to randomise transmissions of the output signal from the transmitter is determined by the length of the counter, the data lines between the random number generator and the counter being gated in order to "fold" the counter such that the effective counter length may be modified in multiples of two.

In alternative embodiments the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from the interrogator in a command.

An up or a down counter may be used whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required, and the output response signal contains identity or field data of a tag or transponder.

In a further aspect of the invention there is provided a transponder for generating an output signal during a waiting period, including means for deriving a random number within the transponder and delivering the random number by way of binary output signals along a plurality of data lines to a counter, characterised in that at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

In one embodiment the transponder includes a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised in that at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period. Other embodiments of the transponder include the features defined in any one of the transponder claims incorporated hereinafter.

In a further aspect of the invention there is provided an identification system comprising an interrogator and a plurality of transponders, the interrogator including a transmitter for transmitting an interrogation signal to the transponders, each transponder including a receiver for receiving the interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation

signal and means for generating the response signal during a waiting period, each transponder having means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, the transponder including a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised in that at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period. Other embodiments of the identification system are defined in any one of the system claims incorporated hereinafter.

The present invention further provided an integrated circuit for use in a transponder of an RFID interrogation system, the integrated circuit comprising a receiver for receiving an interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal, means for generating the response signal during a waiting period and control means for altering the maximum length of the waiting period, characterised by means for deriving a random number within the integrated circuit and delivering the random number by way of binary output signals along a plurality of data lines to a counter and wherein at least one of the data lines is connected to the counter via logic circuitry control of which can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

In one embodiment there is provided a random number generator the binary output signals from which are fed to the inputs of the counter for determining the waiting period, and logic circuitry whereby at least one of the output signals from the random number generator is fed via the logic circuitry to a respective input of the counter, control of the logic circuitry thereby providing means for adjusting the maximum length of the waiting period. Other embodiments of the integrated circuit or transponder chip are incorporated by reference to the integrated circuit claims hereinafter.

This invention provides a method of adjusting the maximum waiting period or number of slots using a minimum number of logic components. Prior art systems use more complex methods using considerably larger logic circuits to store the round size value and required the slot counter to be electrically "re-wired" in order to change the count value. This resulted in increased chip size and power consumption.

The present method provides a simple means of adjusting the round size by "folding" the counter using only few additional gates compared with a non adjustable round size device. This results in decreased chip complexity, simple operation and reduced power consumption which translates into longer read ranges.

DESCRIPTION OF THE DRAWINGS

The invention will be described further, by way of examples, with reference to the accompanying drawings, in which:

Figure 1 is a partial schematic diagram of a logic circuit according to one embodiment of the invention;
Figure 2 is a truth diagram for the gating arrangement shown in Figure 1;
Figures 3, 4 and 5 show the maximum transmit delay for three different Round Sizes and
Figure 6 is a partial schematic diagram of a further embodiment of the invention.

DESCRIPTION OF THE INVENTION

For the purposes of this description a simplified logic circuit figure 1 will be used to illustrate the principle. This simplified logic circuit comprises a 4 bit pseudo-random number generator (PRNG) **10**, a 4 bit down counter **20** and two AND gates **30** and **40**. The PRNG is driven by the system clock on input **11**. The PRNG continuously generates a random number which is presented to the outputs **12**, on binary lines representing weighted binary values 1, 2, 4 and 8. Binary lines 1 and 2 are routed directly to the 1 and 2 preload inputs of down counter **20.** Binary lines 4 and 8 are routed first to one input of each of AND gates **40** and **30** respectively. The second input of each AND gate **41** and **31** respectively, are used to control the Round Size as shown in figure 2. The outputs of each of these AND gates is routed to the binary 4 and binary 8 inputs, **26** and **25** of the 4 bit down counter **20**. Refer now to figure 3. The diagram illustrates a round having a size of 16 time intervals or slots labelled 0...15. Each of these time slots is uniquely identified by a combination of the weighted binary values 1, 2, 4 and 8 appearing on the output **12** or PRNG **10**. For example slot 13 is represented by a combination of 8 + 4 + 1 or written in binary notation 1101. In figure 3, the 16 slots may also be represented by 4 successively concatenated blocks each having 4 time slots giving a total of 16 time slots. Refer again to figure 1, when the chip is enabled the system clock causes the PRNG **10** to generate a random number which is presented to the load inputs of the down counter **20**. Either on receipt of an instruction from an interrogator, or on a stimulus from and internal circuit, the down counter Enable line **23** goes active and causes the down counter **20** to start counting down. The counter decrements for each input pulse from time slot clock **22**. If for example the counter is preloaded with a count of '13', meaning that the chip must wait for 14

intervals before transmitting its data, or that the chip will transmit in slot 13, the counter will decrement to '0' after 14 input pulses from the time slot clock **22**, the down counter **20** will output a trigger pulse **24** which causes the chip to transmit its data. This trigger pulse also connects to pre-load input **21** which causes the down counter **20** to again pre-load a new value from the PRNG **10**. This new value could be for example '3' represented by binary 0011 in which case the down counter will need 4 pulses from the time slot clock before sending the output trigger pulse therefore causing the chip to transmit after a waiting period of 4 time intervals in other words it will transmit in time slot number 4. Refer now to figure 4. If the down counter was preloaded with '13' being slot 13, and the counter has been folded once, in other words the round size is 8, slot 13 corresponds to slot 5; or if the counter has been folded twice for a round size of 4, slot 13 now corresponds to slot 1. The folding mechanism is controlled by gating the '4' and '8' binary control lines by means of AND gate inputs **41** and **31** respectively according to the truth table in figure 2. These control inputs may be derived from an instruction received from an interrogator or they may be derived internal to the chip. The pre-load input **21** only occurs at the time of the first trigger output, thereby allowing a known pre-determined value to determine the maximum time hold-off time on the first transmission to take place after arbitration is enabled. This is further described below.

It will be appreciated that there may be many variants on the implementation described above. For example the random number generator may be of any required length in order to provide the desired degree of randomness. It may also be of any type or configuration. Indeed the random number may be derived from another source such as taking a snapshot of the system clock, or may be a hash value received from the interrogator in a command. The counter may be of any length as required by the transponder chip or system requirements and it may be either an up counter or down counter with the clocking signal causing the counter to either increment or decrement as required. The control input may be stored in a latch which is set by an external instruction from the interrogator and accessed by chip circuitry as required. It may also be derived internally in the chip from other information available to the chip logic, such as by the chip itself determining the degree of congestion.

In one embodiment the reader or interrogator determines the proportion of collisions occurring and the amount of white space occurring and accordingly adjusts the Round Size. As collisions increase proportional to the number of successful reads, the round size should be increased. As the

proportion of white space increases in proportion to the number of successful reads the round size should be decreased.

One method of monitoring congestion might be to count the number of Acknowledgement signals (Next Slot commands in the case of ISO 18000-6) that are transmitted by the interrogator to the tag population to acknowledge the successful reading of tags. A decrease in the number of Acknowledgements could indicate that there is a high number of collisions occurring and therefore the chip needs to increase its maximum hold-off time. An increase in a number of Close Slot commands in the case of ISO 18000-6 slotted Aloha systems would indicate that there are few tags in the field because these commands are only issued when there are empty slots; these Close slot commands being counted and used to determine the relative low level of congestion, allowing the chip to reduce the maximum hold-off time intervals thereby causing the speeding up of the reading of a population of tags. It will be appreciated that other systems may not use specific Close Slot commands but may use another command which serves the same purpose, that is to reduce the amount of unproductive time in tag transmission intervals.

In another aspect of the invention, Tags that have entered a population that have not yet been included in the active group by an interrogator instruction, will have their internal prescaler 60 mechanism (see Figure 6) or parts thereof free running but not transmitting and therefore maintaining a non-synchronised state with other tags. During this state the slot counter **20** will be maintained or held in a known state which may be all zeros or may be in another value. When the tags included in the active population by an interrogator instruction the tag will have a pre-known number of slot interval before it will do its first transmission. In this way it can be arranged that a tag transmission may occur at an early stage in the arbitration cycle thus facilitating reading of small numbers of tags moving at high speed such as on a conveyer belt or in a moving vehicle. Because the prescaler mechanism 60 has not been held in a fixed state, tags will inherently distribute their positions because of the naturally occurring drift in their clock frequencies.

Figure 6 shows a partial schematic diagram of yet another aspect of the invention, features the same as those shown in Figure 1 being represented by identical reference numerals. In this embodiment the PRNG 10 may be switched between a Fast Clock and the Regular System Clock, the outputs of each of which are connected to inputs of respective AND gates 50,52, the other inputs of the AND gates 50,52 being connected to a Ready State signal which is also used to reset the counter 24. The outputs of the AND gates 50,52 are connected to the inputs of an OR gate 54, the output of which

locks the PRNG. The Ready State signal is also passed via an AND gate 56 to an input of a gate 58 which also receives the feedback trigger pulse signal from the output of the counter 20, causing the down counter **20** to again pre-load a new value from the PRNG **10**.

The Fast Clock causes the random number to cycle much more quickly thus providing a better chance of different tags having more widely spaced randomness where tags are introduced to the RF energising field simultaneously and where their internal PRNG circuits are almost in sync. Another aspect of this embodiment is the independent Fast Load circuit which allows the counter 20 to be pre-loaded with a fast random number for the tag's first transmission in an arbitration sequence; thereafter the counter 20 is loaded with the random number generated by the System Clock.

It will be appreciated that the embodiments described here serve only to illustrate the method, system and possible implementation; that the invention is not restricted to these embodiments and that there are many other possible embodiments.

CLAIMS

1. A method of identifying a plurality of transponders in an interrogation process comprising transmitting an interrogation signal to the transponders and receiving a response signal from each transponder at a time within a respective waiting period the maximum duration of which can be adjusted, characterised by creating a plurality of data line signals together defining a random number, feeding said data line signals to a counter for determining the waiting period, and providing at least one of the data lines with logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

2. A method of identifying a plurality of transponders in an interrogation process comprising transmitting an interrogation signal to the transponders and receiving a response signal from each transponder during a respective waiting period the maximum duration of which can be adjusted, the transponder having a random number generator and a counter, characterised by transmitting output signals from the random number generator to respective inputs of the counter for determining the waiting period, at least one of the output signals from the random number generator being fed via logic circuitry to a respective input of the counter and controlling the logic circuitry to adjust the maximum length of the waiting period..

3. A method as claimed in claim 1 or claim 2, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines.

4. A method as claimed in any one of claims 1 to 3, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

5. A method as claimed in claim 4, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

6. A method as claimed in any one of claims 1 to 5, wherein by controlling the logic circuitry the maximum duration of the waiting period is increased or decreased by multiples of 2 or 0.5 respectively.

7. A method as claimed in claim 5, wherein by controlling the logic circuitry the desired Round Size is selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

8. A method as claimed in claim 2, or in any one of claims 3 to 7 when dependent on claim 2, including the step of clocking the random number generator and/or clocking the counter by means of a clock oscillator of the transponder.

9. A method as claimed in claim 8, including causing the transponder to transmit an output signal from its transmitter when the counter has been counted to its terminal count, whereupon the counter loads a fresh or new number from the random number generator for the next count.

10. A method as claimed in claim 8 or claim 9, comprising determining the maximum possible waiting time or maximum possible number of slots over which to randomise transmissions of the output signal from the transmitter by the length of the counter, the data lines between the random number generator and the counter being gated in order "fold" the counter such that the effective counter length may be modified in multiples of two.

11. A method as claimed in claim 1 or any of claims 3 to 10 when dependent on claim 1, including deriving the random number by taking a snapshot of the transponder clock, or by a hash value received from the interrogator in a command.

12. A method as claimed in any one of claims 1 to 11, including using either an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

13. A method as claimed in any one of claims 1 to 12, wherein the output response signal contains identity or field data of a tag or transponder.

14. A transponder for generating an output signal during a waiting period, including means for deriving a random number within the transponder and delivering the random number by way of binary output signals along a plurality of data lines to a counter, characterised in that at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

15. A transponder for generating an output signal during a waiting period, the transponder including a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised in that at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period

16. A transponder as claimed in claim 14 or claim 15, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals.

17. A transponder as claimed in any of claims 14 to 16, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

18. A transponder as claimed in claim 17, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

19. A transponder as claimed in any one of claims 14 to 18, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

20. A transponder as claimed in claim 18, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

21. A transponder as claimed in any one of claims 14 to 20, wherein the transponder dynamically alters the maximum waiting time in response to an instruction from an interrogator.

22. A transponder as claimed in any one of claims 14 to 21, wherein the transponder is adapted to detect either heavy signal congestion or large quiet signal periods and alter the maximum waiting time accordingly.

23. A transponder as claimed in any of claims 14 or 22, wherein the transponder is adapted to alter the maximum waiting time in response to an instruction from the interrogator or in response to external conditions present during the interrogation.

24. A transponder including a receiver for receiving an interrogation signal from an interrogator, a transmitter for transmitting a response signal after receipt of the interrogation signal, means for generating the response signal during a waiting period and a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised in that at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period during interrogation by the interrogator.

25. A transponder as claimed in claim 24 including the features defined in any one of claims 14 to 23..

26. A transponder as claimed in claim 14 or any one of claims 16 to 25 when dependent on claim 14, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

27. A transponder as claimed in any one of claims 14 to 26, wherein the counter is an up or down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

28. A transponder as claimed in any one of claims 14 to 27, including a memory for storing an identity or data field and a modulator for transmitting the identity or data as a message in the output response signal.

29. An identification system comprising an interrogator and a plurality of transponders, the interrogator including a transmitter for transmitting an interrogation signal to the transponders, each transponder including a receiver for receiving the interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal and means for generating the response signal during a waiting period, each transponder having means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, the transponder including a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised in that at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter whereby control of the logic circuitry adjusts the maximum length of the waiting period.

30. An identification system comprising an interrogator and a plurality of transponders, the interrogator including a transmitter for transmitting an interrogation signal to the transponders, each transponder including a receiver for receiving the interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal and means for generating the response signal during a waiting period, each transponder having means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator, the transponders having means for deriving a random number within the transponder and delivering the random number by way of binary output signals along a plurality of data lines to a counter, characterised in that at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

31. An identification system as claimed in claim 29 or claim 30, wherein the transponder includes the features defined in any one of claims 14 to 28.

32. An integrated circuit for use in a transponder of an RFID interrogation system, the integrated circuit comprising a receiver for receiving an interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal, means for generating the response signal during a waiting period and control means for altering the maximum length of the waiting period, characterised by means for deriving a random number within the integrated circuit and delivering the random number by way of binary output signals along a plurality of data lines to a counter and wherein at least one of the data lines is connected to the counter via logic circuitry control of which can block or permit the data line signal to the counter thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period.

33. An integrated circuit for use in a transponder including a receiver for receiving an interrogation signal, a transmitter for transmitting a response signal after receipt of the interrogation signal and means for generating the response signal during a waiting period and control means for altering the maximum length of the waiting period during interrogation of the transponder by the interrogator, a random number generator the binary output signals from which are fed to the inputs of a counter for determining the waiting period, characterised by logic circuitry whereby at least one of the output signals from the random number generator is fed via the logic circuitry to a respective input of the counter, control of the logic circuitry thereby providing means for adjusting the maximum length of the waiting period.

34. An integrated circuit as claimed in claim 32 or claim 33, wherein the logic circuitry comprises one or more logic gates, the number of logic gates being less than the number of data lines for the binary output signals to the counter.

35. An integrated circuit as claimed in any one of claims 32 to 34, wherein the waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period.

36. An integrated circuit as claimed in claim 35, wherein there is a minimum Round Size and at least one larger Round Size, the or each larger Round Size consisting of a combination of minimum Round Sizes, whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used.

37. An integrated circuit as claimed in any one of claims 32 to 36, wherein the logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively.

38. An integrated circuit as claimed in claim 36, wherein the logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of minimum Round Sizes to be combined, the different Round Sizes available being related to one another by factors or multiples of 2 or 0.5.

39. An integrated circuit as claimed in claim 32 or any of claims 34 to 38 when dependent on claim 32, wherein the random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator.

40. An integrated circuit as claimed in any one of claims 32 to 39, wherein the counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required.

41. An integrated circuit as claimed in any one of claims 32 to 40, including a memory for storing an identity or data field and a modulator for transmitting the data in the output response signal.

ABSTRACT

Arbitration Management Method and System

The invention describes an arbitration management method and system for use in identifying RFID transponders or tags which each transmit a response signal to a reader within a respective waiting period the maximum duration of which can be adjusted. The maximum duration is determined by a random number transmitted to a counter (20) along a number of data lines (1,2,4,8), at least one of the data lines (4,8) being provided with logic gates (40,30) which block or permit data line signals reaching the binary inputs (26,25) of the counter to control the maximum length of the waiting period.

Figure 1

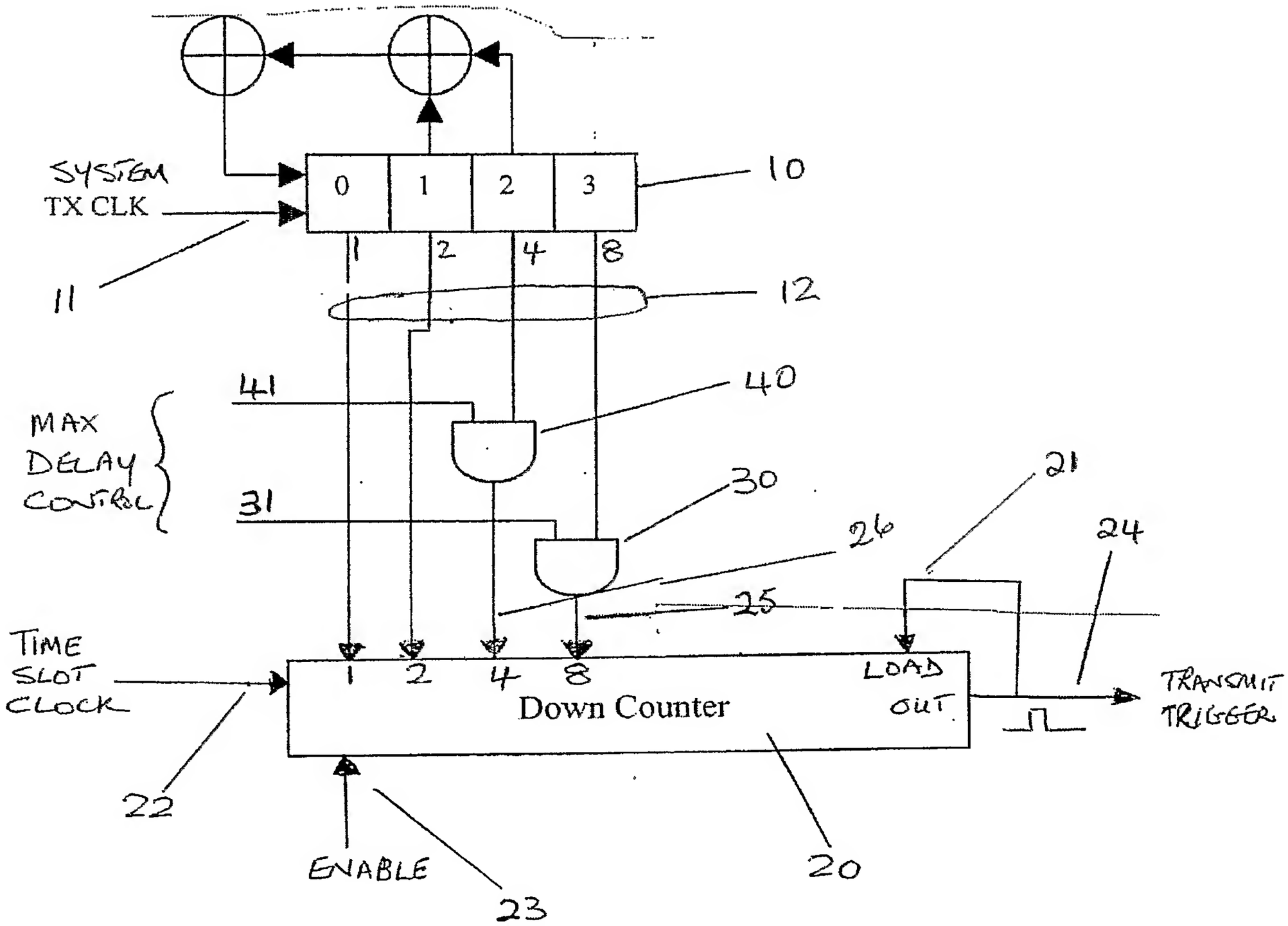
SYSTEM
TX CLK
0
1
2
3
10
11
1
2
4
8
12
41
40
MAX
DELAY
CONTROL
31
30
21
26
24
25
TIME
SLOT
CLOCK
1
2
4
8
LOAD
OUT
TRANSMIT
TRIGGER
Down Counter
22
ENABLE
23
20

Figure 1.

Input 41	Input 31	Round Size
1	1	16
1	0	8
0	0	4

Figure 2.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 3. Maximum transmit delay 16 time periods (Round Size = 16)

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15

Figure 4. Maximum transmit delay 8 time periods (Round Size = 8)

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

Figure 5. Maximum transmit delay 4 time periods (Round Size = 4)

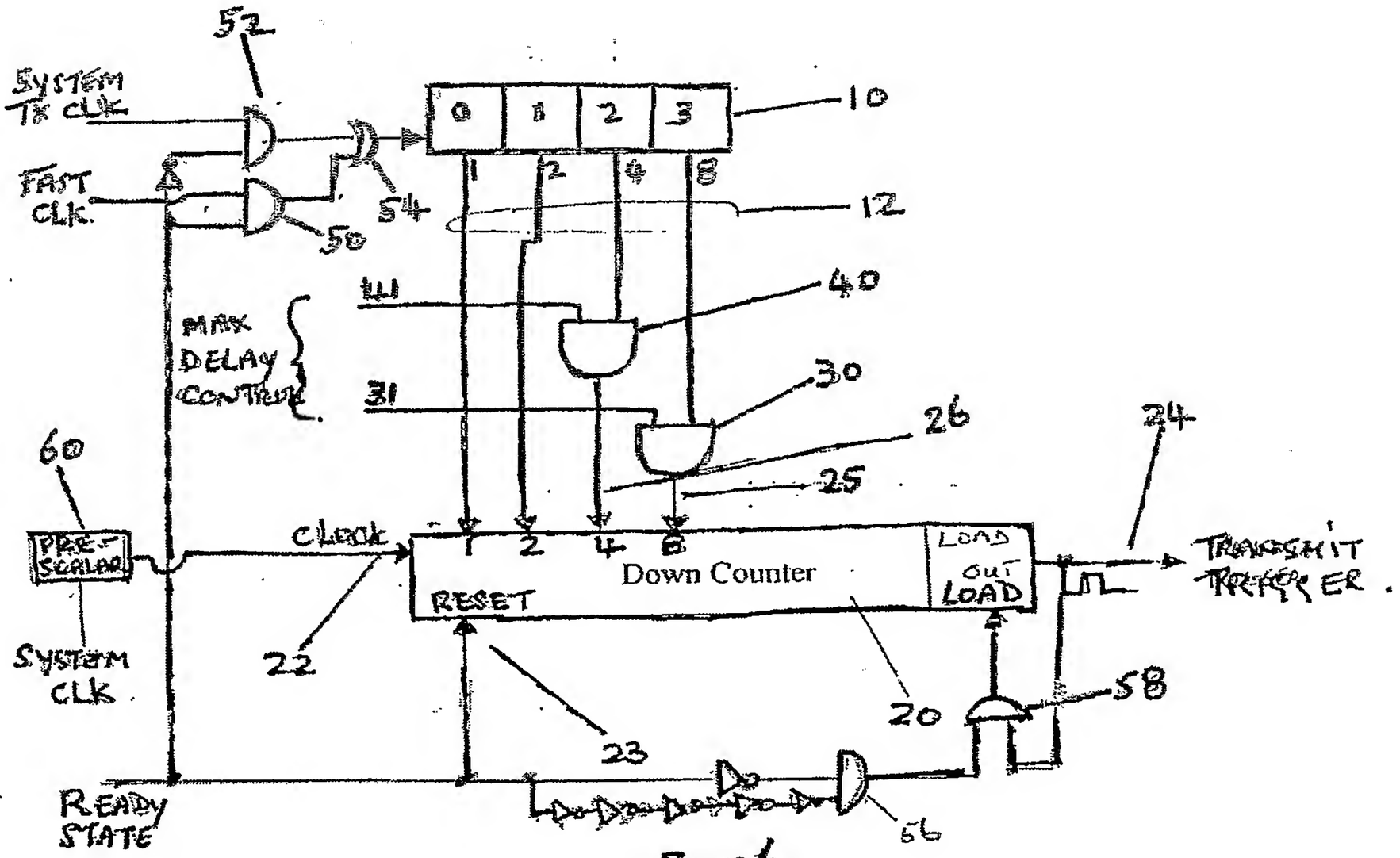
52
SYSTEM TX CLK
FAST CLK.
54
50
0
1
2
3
10
1
2
4
8
12
11
40
MAX DELAY CONTROL
31
30
26
25
24
60
PRE-SCALAR
CLOCK
1
2
4
8
Down Counter
LOAD
OUT
LOAD
RESET
TRANSMIT TRIGGER
SYSTEM CLK
22
20
58
23
READY STATE
56

Figure 6